CLAIMS

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1. A processor comprising:

a first plurality of threads, each of said first plurality of threads comprising one of a second plurality of processing units;

each of said first plurality of threads receiving a respective one of a third plurality of issue groups, wherein each of said respective one of said third plurality of issue groups belongs to a respective one of a fourth plurality of instruction packets;

said processor executing said third plurality of issue groups in a single clock cycle, wherein each of said third plurality of issue groups is executed in a respective one of said second plurality of processing units.

2. The processor of claim 1 wherein each of said first, second, third, and fourth pluralities is equal to two.

3. The processor of claim 1 wherein each of said fourth plurality of instruction packets consists of two issue groups.

4. The processor of claim 3 wherein each of said fourth plurality of instruction packets is 128 bits wide.

5. The processor of claim 4 wherein a first one of said two issue groups is 64 bits wide and a second one of said two issue groups is 48 bits wide.

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6. The processor of claim 4 wherein a first one of said two issue groups is 48 bits wide and a second one of said two issue groups is 64 bits wide.

7. The processor of claim 1 wherein each of said fourth plurality of instruction packets resides in a respective instruction cache and is addressed by a respective program counter.

8. The processor of claim 1 wherein each of said first, second, third, and fourth pluralities is equal to four.

9. A method comprising steps of:

dividing a first instruction packet into a first packet first issue group and a first packet second issue group;

dividing a second instruction packet into a second packet first issue group and a second packet second issue group;

providing said first packet first issue group to a first thread having a first thread processing unit, and providing said second packet first issue group to a second thread having a second thread processing unit, whereby said first packet first issue group and said second packet first issue group are executed in a first clock cycle.

10. The method of claim 9 further comprising a step of providing said first packet second issue group to said first thread having said first thread processing unit, and providing said second packet second issue group to said second thread having said

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second thread processing unit, whereby said first packet second issue group and said second packet second issue group are executed in a second clock cycle.

11. The method of claim 9 wherein each of said first and second instruction packets consists of 128 bits.

12. The method of claim 11 wherein said first packet first issue group consists of 64 bits and said first packet second issue group consists of 48 bits.

13. The method of claim 11 wherein said first packet first issue group consists of 48 bits and said first packet second issue group consists of 64 bits.

14. The method of claim 11 wherein said second packet first issue group consists of 64 bits and said second packet second issue group consists of 48 bits.

15. The method of claim 11 wherein said second packet first issue group consists of 48 bits and said second packet second issue group consists of 64 bits.

16. The method of claim 9 wherein each of said first and second instruction packets consists of 256 bits.

17. The method of claim 16 wherein said first packet first issue group consists of 128 bits and said first packet second issue group consists of 112 bits.

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18. The method of claim 16 wherein said first packet first issue group consists of 112 bits and said first packet second issue group consists of 128 bits.

19. The method of claim 16 wherein said second packet first issue group consists of 128 bits and said second packet second issue group consists of 112 bits.

20. The method of claim 16 wherein said second packet first issue group consists of 112 bits and said second packet second issue group consists of 128 bits.

21. A method comprising steps of:

dividing each one of a first plurality of instruction packets into a second plurality of issue groups;

providing each one of said second plurality of issue groups, in one of a third plurality of clock cycles, to a respective thread having a respective processing unit;

executing said first plurality of instruction packets in said third plurality of clock cycles.

22. The method of claim 21 wherein each of said first, second, and third pluralities is equal to two.

23. The method of claim 21 wherein each one of said first plurality of instruction packets consists of two issue groups.

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24. The method of claim 23 wherein each one of said first plurality of instruction packets is 128 bits wide.

25. The method of claim 24 wherein a first one of said two issue groups is 64 bits wide and a second one of said two issue groups is 48 bits wide.

26. The method of claim 24 wherein a first one of said two issue groups is 48 bits wide and a second one of said two issue groups is 64 bits wide.

27. The method of claim 21 wherein each one of said first plurality of instruction packets resides in a respective instruction cache and is addressed by a respective program counter.

28. The method of claim 21 wherein said first plurality is equal to four, and wherein each of said second and third pluralities is equal to two.